Nakamigawa does not disclose the feature of the last paragraph of claim 1, as the Examiner admits. The Examiner relies on Hirano for this feature.

Hirano typifies the non-WCSP[1] prior art that uses wire bonding (the wires 10 of Hirano). Unlike Nakamigawa, Hirano has the chip contacts 8 on the side of the chip facing away from the substrate 1A and solder bumps 12 (Nakamigawa's corresponding contacts, 10, are on the *same* side as Nakamigawa's solder bumps 12). Wire bonding results in a thick package, as described by the Applicant at page 4, lines 4-9.

Claim 1. In the Applicant's claim 1, there are no bonding wires and all of the components are on the same side. Claim 1 recites *a first main surface on which a plurality of electrode pads are provided ... an insulating film formed on a surface of said extension portion and said first main surface such that a part of each of said electrode pads is exposed.* That is, the insulating film covers the front surface of the chip and the adjacent surface of the surrounding extension portion. Therefore, all components are on the same side, according to claim 1.

The Hirano reference shows a different structure. This is discussed below.

Motivation. With respect, the rejection does not present any cogent motivation for the person of ordinary skill to have combined the references, which of different types and possibly not even compatible. The Examiner is invited to consider:

(1) The Applicant sees that Hirano's chip 7B could not be flipped over to have the chip contacts 8 facing the board 1A, because those contacts would short out against the various conductors below, and so would require an additional layer of insulation and wiring beyond what is already provided. Thus, Hirano would become complicated and therefore would not benefit from the chip orientation of Nakamigawa.

Moreover, flipping the chip would be contrary to the reference itself. Hirano teaches that its disclosed "technique [is] effective when used for a semiconductor device having a *face up structure*" (col. 1, line 8; emphasis added) and teaches that the face-up structure "can be produced at a low cost using an existing plant [and] are most popular" (col. 1, line 21).

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[1] Wafer-level Chip Size Package (page 1, line 13).

Conversely, it has not been established that Nakamigawa would benefit from the arrangement of the solder balls (external terminals) 12[2] of Hirano. Hirano does not even disclose more than a single solder ball near the edges of the chip, and to achieve the arrangement of Hirano, Nakamigawa would need to add additional solder balls (but there is no teaching toward this) and arrange them in the manner of Hirano (there is no teaching toward this either).

(2) Nakamigawa's stated object is preventing the breakage of a connecting portion between the printed board and external electrodes. A resin layer is provided on the substrate for aligning the thermal expansion of the substrate and printed board, and in particular the external electrodes are provided on the resin layer. This is completely unrelated to Hirano's objects, and Hirano already has an adhesive layer of epoxy or polyimide between the chip and substrate (Figs. 13 and 15; col. 6, line 38) which will provide mechanical isolation and reduce stress. (If more stress isolation were desired (not taught by the reference), it would be much easier to make the layer 9 thicker than to completely rebuild the structure of Hirano to be like that of Nakamigawa.)

(3) The Examiner asserts that it would have been obvious to combine the references because combining "maximizes the area of a semiconductor device," that is, the area of the chip 1 of Nakamigawa. However, the Examiner does not explain *why* making the chip 1 larger in area would be advantageous. Also, the motivation asserted by the Examiner is *directly contrary* to the object of Hirano, which is "a technique which permits ... a semiconductor chip *smaller* in external size than an ordinary semiconductor chip" (Abstract, line 1, emphasis added; see also col. 2, lines 33, 38, 44).

Advantages. The subject matter of instant claim 1 provides a greater degree of design freedom regarding the disposal pitch, disposal positions, and so on of the external terminals (exemplified by terminals 48/47(a) in Fig. 1). Improvements in operational speed, functional sophistication, number of functions, compactness, and operational reliability can also be

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[2] The Examiner asserts (page 3, line 3) that the bump lands 4 of Hirano anticipate the claimed external terminal, but the bump lands 4 are not external; they are buried. This is clearly shown in Fig. 4. Only the solder bumps 12 are external.

achieved with the Applicant's claimed subject matter. The applied references do not disclose or suggest the Applicant's advantages.

Withdrawal of the rejection is requested.

[4-5] Claim 4 is rejected under § 103 over Nakamigawa in view of Hirano and Jackson US '930. This rejection is respectfully traversed on the grounds set out above and the dependence of claim 4.

[6] Claim 7 is rejected under § 103 over Nakamigawa in view of Hirano and Torres US '213. This rejection is respectfully traversed on the grounds set out above, the dependence of claim 7, and the reference itself.

With respect, the Examiner has misconstrued the applied 'A' and 'B' as boundaries. They are actually radii. The Examiner is invited to note col. 3, line 61 where A' and B' are named "axis" and col. 3, line 66, stating "axis A' and axis B' may define an arc of varying radius." There is no mention of any boundary, and therefore it appears that the Examiner has misconstrued the lines indicating the arcs. Withdrawal of the rejection is requested.

[7] Claims 8 and 9 were rejected under § 103 over Nakamigawa in view of Hirano and Ma US '469. This rejection is respectfully traversed on the grounds set out above, the dependence of the claims, and the following argument.

The Examiner does not explain how the materials 118 and 112 of Ma are to be applied to the other two references. Since Nakamigawa is the base reference, the Applicant assumes that Ma is applied to it: but to which layers? The Applicant notes that Nakamigawa's abstract discloses that layer 21 is of resin, but not the extension section 9.

Because the goal of Nakamigawa is to avoid strain ("warp/deformation"), using materials of different shrinkage would be contrary to this reference.

The reference does not disclose two materials with different molding shrinkage. Only resin has molding shrinkage; silicon nitride and silicon dioxide do not, because they are crystalline and never are molded.

The specific features of claim 9 are not disclosed, and the Examiner asserts that these features would be obvious for "adequate mechanical rigidity, ... protection for the semiconductor chip, and ... surface area." With respect, none of these asserted advantages has been related to the coefficient of thermal expansion, and the Applicant is unaware of any functional relationship whatsoever between thermal expansion and the asserted advantages. As to the modulus of elasticity, there is no direct correlation or any reasoned argument, as required by the MPEP.

Withdrawal of the rejection is requested.

In view of the present amendments, withdrawal of the rejections, and allowance, are requested.

Respectfully submitted,

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